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Our Case No.10736/9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Najam, et al.

Serial No. 09/858,308

Filing Date: May 15, 2001

For APPARATUS AND METHOD FOR INTERCONNECTING A PROCESSOR TO CO-PROCESSORS USING SHARED MEMORY

Examiner Shane F. Gerstl

Group Art Unit No. 2183

RESPONSE AND AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In reply to the Office Action dated April 1, 2004, please enter the following amendment:

In the Title:

On the cover sheet and on page 1, line 1 of the Specification, please change the Title as follows (the changes on these paragraphs are shown with ~~strikethrough~~ for deleted matter and underlines for added matter):

APPARATUS AND METHOD FOR INTERCONNECTING A PROCESSOR TO CO-PROCESSORS USING A SHARED MEMORY AS THE COMMUNICATION INTERFACE

In the Drawings:

Please replace figures 3 and 15 in their entirety with the replacement figures 3 and 15 in compliance with 37 C.F.R. 1.84(p)(5) provided herewith.

In the Specification:

Please amend Paragraph numbers 2-4 and 74 as follows (the changes on these paragraphs are shown with ~~strikethrough~~ for deleted matter and underlines for added matter):

[0002] U.S. Pat. Application Ser. No. ~~_____~~ 09/858,309, "EDGE ADAPTER APPARATUS AND METHOD", (Attorney Ref. No. 10736/6), filed herewith;

[0003] U.S. Pat. Application Ser. No. ~~_____~~ 09/858,323, "EDGE ADAPTER ARCHITECTURE APPARATUS AND METHOD", (Attorney Ref. No. 10736/7), filed herewith;

[0004] U.S. Pat. Application Ser. No. ~~_____~~ 09/858,324, "APPARATUS AND METHOD FOR INTERFACING WITH A HIGH SPEED BI-DIRECTIONAL NETWORK", (Attorney Ref. No. 10736/8), filed herewith.

[0074] The DPSSRAM blocks 216A, 216B are also coupled with the daughter card 204 via the DPSSRAM daughter card interfaces 232A, 232B. In one embodiment, the DPSSRAM daughter card interface 232A, 232B are each at least 64 bits wide and operate at a frequency of at least 50 MHz. The SRAM control logic ~~328A, 328B228A, 228B~~ 228A, 228B, 328 is coupled with the daughter card 204 via SRAM control logic daughter card interfaces 234A, 234B. In one embodiment, the SRAM control logic 228A, 228B, 328 is a custom

designed device using a CMOS Programmable Logic Device ("CPLD"). Operation of the SRAM control logic 228A, 228B, 328 is described in more detail below.

Please amend the Abstract as follows (the changes on these paragraphs are shown with ~~strikethrough~~ for deleted matter and underlines for added matter):

An apparatus and method for interfacing a processor to one or more co-processors interface ~~is disclosed. The apparatus~~ provides a dual ported memory to be used as a message passing buffer between the processor and the ~~co-processor~~ co-processors. Both the processor and co-processors can ~~interface~~ connect asynchronously to the dual ported memory. Control logic monitors activity by the processor to alert the co-processors of communications by the processor written to the memory and otherwise ~~allow~~ allows the processor and co-processors to think they are interfacing directly with one another.